CLAIMS

What is claimed is:

1. A hot swap protection circuit for an integrated circuit being plugged into a powered-up system, comprises:

a first circuit for detecting a hot swap condition;

a second circuit coupled to the first circuit for preventing a pn junction diode in a pull-up transistor from going into a forward bias condition; and

a third circuit coupled to the first and second circuits for preventing the pull-up transistor from turning on during the hot swap condition.

2. The circuit of claim 1, wherein the circuit for detecting comprises detecting a beginning and an ending of the hot swap condition.

3. The circuit of claim 1, wherein the first circuit comprises a transistor having a gate coupled to an input/output voltage supply during the hot swap and said transistor further having a drain coupled to a pad that is coupled to a signal line of the powered-up system during the hot swap.

4. The circuit of claim 3, wherein the second circuit disconnects the NWELL of the pull-up transistor from the input/output voltage supply during the hot swap condition providing isolation of the NWELL from the input/output voltage supply during the hot swap condition.

5. The circuit of claim 4, wherein the second circuit further charges the NWELL to the voltage level of the signal line during the hot swap condition to prevent the pn junction diode from going into a forward bias condition.

6. The circuit of claim 1, wherein the pull-up transistor is coupled to a pad of the integrated circuit.

7. The circuit of claim 1, wherein the integrated circuit forms a part of a printed circuit board being plugged into the powered-up system.

8. The circuit of claim 1, wherein the pull-up transistor is a pmos transistor.

9. A method of protecting a powered-up system during the insertion of an integrated circuit, comprising the steps of:

detecting a hot swap condition;

preventing a forward bias condition in a pn junction diode of a pull-up transistor of the integrated circuit during the hot swap condition; and

biasing the pull-up transistor coupled to a pad of the integrated circuit to remain turned off during the hot swap condition.

10. The method of claim 9, wherein the step of detecting comprises the step of detecting the start of the hot swap condition when a voltage at a pad of the integrated circuit is a predetermined amount above an input/output supply voltage and further comprises the step of detecting the end of the hot swap condition when the input/output supply voltage is within a predetermined amount below the voltage at the pad.

11. The method of claim 9, wherein the pull-up transistor forms a portion of the first circuit.

12. A method of protecting a powered-up system during the insertion of a printed circuit board containing an integrated circuit, comprising the steps of:

detecting a hot swap condition;

isolating an nwell of a pmos pull-up transistor from a power source of the powered-up system during the hot swap condition; and

preventing the pmos pull-up transistor coupled to a pad of the integrated circuit from turning on during the hot swap condition.

13. The method of claim 12, wherein the step of detecting comprises the step of detecting a beginning and an ending of the hot swap condition.

14. The method of claim 12, wherein the step of isolating comprises disconnecting the NWELL of the pull-up transistor from the power source of the powered-up system during the hot swap condition providing isolation of the NWELL from the power source during the hot swap condition.

15. The method of claim 12, wherein the step of isolating comprises the step of charging the NWELL to the voltage level of a signal line of the powered-up system during the hot swap condition to prevent the pn junction diode from going into a forward bias condition.